UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,752	10/06/2003	Jeffrey H. Burns	DP-310264	2820

22851 7590 12/05/2008

DELPHI TECHNOLOGIES, INC.
M/C 480-410-202
PO BOX 5052
TROY, MI 48007

EXAMINER	
CUTLER, ALBERT H	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
12/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,752	BURNS, JEFFREY H.	
	Examiner	Art Unit	
	ALBERT H. CUTLER	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8,9 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,9 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communication filed on September 9, 2008.

Response to Arguments

2. Applicant's arguments with respect to claims 1-5, 8, 9 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 2001/0050717) in view of Bauer et al. (US 6,621,616).

Consider claim 1, Yamada et al. teaches:

An optical sensor circuit assembly(figure 2), comprising:

an optically transmissive substrate(filter, 24), including filter material(The optically transmissive substrate(24) is a filter, paragraph 0041);

an electrical circuit("stepped wiring board", 21) on a first surface of the optically transmissive substrate(24, see figure 2), the electrical circuit(21) including electrically conductive leads(See figure 5B, paragraphs 0060-0062. The electrical circuit(21) has conductive leads(21a) which provide an electrical connection to a projecting electrode(27).);

an integrated circuit including an optical imaging element("image pick-up semiconductor", 4) located on a face of the integrated circuit(4) facing the substrate and electrically conductive pads(27) on a face(i.e. top face) of the integrated circuit(The integrated circuit is an "image pick-up semiconductor" with an image pickup region denoted by 22 of figure 2, and a peripheral portion containing conductive pads(27) on a face thereof and detailed further in figure 5B.), the optical imaging element(4) spaced away from the first surface(i.e. bottom surface) of the optically transmissive substrate(24, see figure 2); and

an optically transmissive medium filling space between the integrated circuit(4) and the optically transmissive substrate(Yamada teaches an image pickup opening(22) formed in the electrical circuit(21, paragraph 0041, see figure 2). As the integrated circuit(4) is a CMOS "image-pickup semiconductor", the space between the integrated circuit(4) and the optically transmissive substrate(24) must comprises an optically transmissive medium such that light reaches the image pickup device(4). For instance, air is an optically transmissive medium.);

the integrated circuit(4) electrically coupled to and mounted directly on the electrical circuit(21) disposed on the said substrate(24) by an electrical connection between the electrically conductive pads(27) on the face of the integrated circuit(4) and the electrically conductive leads(21a, figure 5B) of the electrical circuit(21) on the substrate(24, paragraphs 0042-0043, 0060-0062).

However, Yamada et al. does not explicitly teach that the optically transmissive medium acts as an environmental seal for the face of the integrated circuit facing the substrate.

Bauer et al. similarly teaches an optical sensor circuit assembly(figure 10) with an integrated circuit including an optical imaging element(optical sensor, 22) spaced away from a surface of an optically transmissive substrate(transparent base substrate, 140).

However, in addition to the teachings of Yamada et al., Bauer et al. teaches that an optically transmissive medium(transparent curable resin, 154) filling the space between the integrated circuit(22) and the optically transmissive substrate(140) acts as an environmental seal for the face of the integrated circuit facing the substrate(See column 14, lines 4-12. The transparent curable resin (154) is coated around the sensor (22), and thus acts as an environmental seal for the face of the integrated circuit facing the substrate. See figure 10.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the optically transmissive medium taught by Yamada et al. comprise a transparent curable resin as taught by Bauer et al. which acts as an

environmental seal for the face of the integrated circuit facing the substrate for the benefit of maintaining the compact nature and ease of manufacture of the optical sensor circuit assembly while better protecting the optical sensor (Bauer et al., column 2, lines 28-32).

Consider claim 8, and as applied to claim 1 above, Yamada et al. further teaches that the optical imaging element(see "image pick-up semiconductor", 4) is electrically coupled to the electrical circuit(21) by electrically conductive bumps(32a) disposed between the leads(21a) and the pads(27, see figure 5B, paragraphs 0060-0062).

Consider claim 9, and as applied to claim 1 above, Yamada et al. further teaches at least one optical element(lens, 2) positioned to direct electromagnetic radiation through said substrate and filter material(24) and to said optical imaging element(4, see figure 2, paragraph 0041).

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. in view of Bauer et al. as applied to claim 1 above, and further in view of Melman et al.(US 6,564,018).

Consider claim 2, and as applied to claim 1 above, Yamada et al. teaches that the optically transmissive substrate(24) includes filter material(paragraph 0041). However, the combination of Yamada et al. and Bauer et al. does not explicitly teach the structure of said filter material.

Melman et al. is similar to Yamada et al. in that Melman et al. teaches an optical sensor circuit assembly(figures 1-9b), comprising an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49), and an optical imaging element("sensor", 116, column 6, line 52, figure 8c) coupled to said substrate(sensor(116) is coupled to filter material(820) with glue layer(800), see figure 8c). Melman et al. also similarly teaches that the optically transmissive substrate includes filter material(cover glass(106) has an antireflective coating(816) and an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6).

However, in addition to the teachings of the combination of Yamada et al. and Bauer et al., Melman et al. teaches that said filter material is embedded in said substrate("deposited on internal surface(818, i.e. embedded) of glass cover(806, i.e. said substrate)", column 7, lines 3-5).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the filter material taught by the combination of Yamada et al. and Bauer et al. comprise embedded filter material as taught by Melman et al. for the benefit of preventing excess ghosting and scattered light as is caused by internal reflections of optically transmissive substrates, reducing the number of pieces of the optical sensor circuit assembly, preventing damage to the filter material due to the cleaning of the separate lens module, and correcting color and/or contrast distortion(Melman et al., column 2, lines 1-24, column 6, line 44 through column 7, line 2).

Consider claim 3, and as applied to claim 1 above, Yamada et al. teaches that the optically transmissive substrate(24) includes filter material(paragraph 0041). However, the combination of Yamada et al. and Bauer et al. does not explicitly teach the structure of said filter material.

Melman et al. is similar to Yamada et al. in that Melman et al. teaches an optical sensor circuit assembly(figures 1-9b), comprising an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49), and an optical imaging element("sensor", 116, column 6, line 52, figure 8c) coupled to said substrate(sensor(116) is coupled to filter material(820) with glue layer(800), see figure 8c). Melman et al. also similarly teaches that the optically transmissive substrate includes filter material(cover glass(106) has an antireflective coating(816) and an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6).

However, in addition to the teachings of the combination of Yamada et al. and Bauer et al., Melman et al. teaches that said filter material is dispersed in said substrate("Instead of using the IR coating an IR absorbing glass may be used(i.e. the IR material is dispersed in the substrate)", column 7, lines 13-14.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the filter material taught by the combination of Yamada et al. and Bauer et al. comprise dispersed filter material as taught by Melman et al. for the benefit of preventing excess ghosting and scattered light as is caused by internal reflections of optically transmissive substrates, reducing the number of pieces of the optical sensor circuit assembly, preventing damage to the filter material due to the

cleaning of the separate lens module, and correcting color and/or contrast distortion(Melman et al., column 2, lines 1-24, column 6, line 44 through column 7, line 2).

Consider claim 4, and as applied to claim 1 above, Yamada et al. teaches that the optically transmissive substrate(24) includes filter material(paragraph 0041). However, the combination of Yamada et al. and Bauer et al. does not explicitly teach the structure of said filter material.

Melman et al. is similar to Yamada et al. in that Melman et al. teaches an optical sensor circuit assembly(figures 1-9b), comprising an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49), and an optical imaging element("sensor", 116, column 6, line 52, figure 8c) coupled to said substrate(sensor(116) is coupled to filter material(820) with glue layer(800), see figure 8c). Melman et al. also similarly teaches that the optically transmissive substrate includes filter material(cover glass(106) has an antireflective coating(816) and an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6).

However, in addition to the teachings of the combination of Yamada et al. and Bauer et al., Melman et al. teaches that said filter material is a thin film layer on the substrate(The Anti-reflective portion on the filter material(816) is applied as a coat(i.e. a thin film layer) on the surface of the substrate(806), column 6, lines 57-65).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the filter material taught by the combination of

Yamada et al. and Bauer et al. comprise a thin film layer as taught by Melman et al. for the benefit of preventing excess ghosting and scattered light as is caused by internal reflections of optically transmissive substrates, preventing damage to the filter material due to the cleaning of the separate lens module, and correcting color and/or contrast distortion(Melman et al., column 2, lines 1-24, column 6, line 44 through column 7, line 2).

Consider claim 5, and as applied to claim 4 above, Yamada et al. teaches that the optically transmissive substrate(24) includes filter material(paragraph 0041). However, the combination of Yamada et al. and Bauer et al. does not explicitly teach the structure of said filter material.

However, Melman et al. further teaches that said thin film layer(816) further comprises material having antireflective properties(column 6, lines 57-65).

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. in view of Bauer et al. as applied to claim 1 above, and further in view of Wolterink et al.(US 2006/0044450).

Consider claim 21, and as applied to claim 1 above, Yamada et al. further teaches a lens mount(3) supporting a lens(2). Yamada et al. also teaches that the lens(2) is situated opposite the first surface(see figure 2). However, the combination of Yamada et al. and Bauer et al. does not explicitly teach that the lens mount is coupled

to a second surface of the optically transmissive substrate opposite the first surface of the optically transmissive.

Wolterink et al. similarly teaches an optical sensor circuit assembly(figures 8a-8e) which contains an optically transmissive substrate in the form of an IR filter(236), and that an image sensor(215) is connected to a first side of the optically transmissive substrate(paragraph 0063). Wolterink et al. likewise teaches a lens mount(260) which positions a lens(270) opposite an image sensor(figures 8a-8e).

However, in addition to the teachings of the combination of Yamada et al. and Bauer et al., Wolterink teaches that the lens mount(260) is coupled to a second surface of the optically transmissive substrate(236) opposite the first surface of the optically transmissive(see figures 8a-8e).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the optically transmissive substrate taught by the combination of Yamada et al. and Bauer et al. extend the entire width of the optical sensor circuit assembly as taught by Wolterink et al., and have the lens mount taught by Yamada et al. attached to the surface of the optically transmissive substrate opposite the first surface as taught by Wolterink et al. for the benefit of simplifying the manufacturing process and thus achieving an efficient mass production operation while maintaining a high positioning accuracy(Wolterink et al., paragraphs 0005-0006).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALBERT H. CUTLER whose telephone number is (571)270-1460. The examiner can normally be reached on Mon-Thu (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

/Sinh N Tran/
Supervisory Patent Examiner, Art Unit 2622